UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,019	06/08/2001	Seiichi Mori	209665US-2	7457

22850 7590 09/02/2003

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
PHAM, HOAI V

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/876,019	MORI, SEIICHI	
	Examiner	Art Unit	
	Hoai V Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *7-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *29 May 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities:

"wherein two kinds of transistors, thickness of the two kinds of transistors" should be changed to --wherein two kinds of gate insulating of transistors, thickness of the two kinds of gate insulating of transistors-- for clarifying the scope of the invention.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakagami [U.S. Pat. 6,281,050] newly cited.

With respect to claim 1, Sakagami (fig. 32) discloses a semiconductor memory integrated circuit comprising:

a semiconductor substrate (210);

a device isolation insulating film (236) buried in grooves formed into said semiconductor substrate;

a cell array having an arrangement of electrically erasable and programmable nonvolatile memory cells made by stacking floating gates (216, 238) and control gates (252) on said semiconductor substrate; and

a peripheral circuit disposed around said cell array on said semiconductor substrate, wherein the bottom layer (216, 238) of said floating gates of the nonvolatile memory cells and the bottom layer (252) of gate electrodes of transistors in the peripheral circuit being maintained in self alignment with said device isolation insulating film (236), N type impurities being doped into the gate electrodes of NMOS transistors and P type impurities being doped into the gate electrodes of PMOS transistors in the peripheral circuit (see col. 14, lines 1-5).

Note that process limitation (at least the bottom layer of said floating gates of said nonvolatile memory cells and at least the bottom layer of gate electrodes of transistors in said peripheral circuit being formed **before** said device isolation insulating film is buried.) do not carry weight in a claim drawn to structure. *In re Thorpe*, 227 USPQ 964 (Fed. Cir. 1985). In addition, a "product by process" limitation is directed to the product per se, no matter how actually made, in re Hirao, 190 USPQ 15 and 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90; and *In re Marosi et al.*, 218 USPQ 289; all of which made clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product by a new

method is not patentable as a product, whether claimed in "product by process" claims or not.

With respect to claim 2, Sakagami (fig. 32) discloses that wherein two kinds of gate insulating of transistors (246 and 250), thickness of the two kinds of gate insulating of transistors (246 and 250) being different from each other, are arranged in the peripheral circuit (see fig. 32 and col. 13, lines 24-25 and lines 44-46).

With respect to claims 3-5, Sakagami (fig. 32) discloses that phosphorus is doped into the floating gates (238) (see col. 12, lines 63-64) and arsenic is doped into the gate electrodes of NMOS transistor in the peripheral circuit (see col. 14, lines 3-4) and a p-type impurity is doped into the gate electrodes of PMOS transistors in the peripheral circuit (see col. 14, lines 4-5).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakagami [U.S. Pat. 6,281,050] newly cited as applied to claim 1 above, and further in view of Ahimizu et al. [U.S. Pat. 6,342,715] previously applied.

Sakagami substantially discloses all the limitation as claimed above. Sakagami also discloses that the floating gates of the nonvolatile memory cells comprise of a first-layer gate electrode material film (216) in self alignment with the device isolation insulating film (236) and a second-layer gate electrode material film (238) stacked on the first gate electrode material film, the control gates comprise of a third-layer electrode material film (252). Sakagami does not teach the gate electrodes in said peripheral circuit have a three-layered structure including said first- to third-layer. However, Ahimizu et al. discloses the gate electrodes in said peripheral circuit have a three-layered structure including said first- to third-layer (35L, 35U, 37) gate electrode material films (fig. 13B). Therefore, it would have been obvious to one of ordinary skill in the art to modify the gate electrodes in said peripheral circuit of Sakagami by forming three layered structure including the first- to third-layer gate electrode material films as set forth above because according to Ahimizu et al., such gate electrode structure would enable the transistor constituting the peripheral circuit to be formed in manufacturing processes similar to those of memory cell transistor (see col. 19, lines 32-35).

Response to Arguments

6. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

8. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai V Pham whose telephone number is 703-308-6173. The examiner can normally be reached on 7:30A.M. - 6:00P.M..

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 703-308-4918. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

11. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HP
Hoai Pham
August 20, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800